NTSC Color TV Signal Encoder

BA7230LS

The BA7230LS comprises an RGB signal matrix circuit, balanced modulator circuit (rectangular 2-phase modulation), oscillator circuit (VCXO) for a 3.58MHz subcarrier synchronized with video input burst signals, luminosity and color difference signal mixing circuit, and a high speed switch for selecting composite signals of video input and RGB input. RGB signals, synch signals, $\overline{BFP}$ (burst flag pulses), $\overline{PCP}$ (pedestal clamp pulses) are input, and an NTSC composite signal is output.

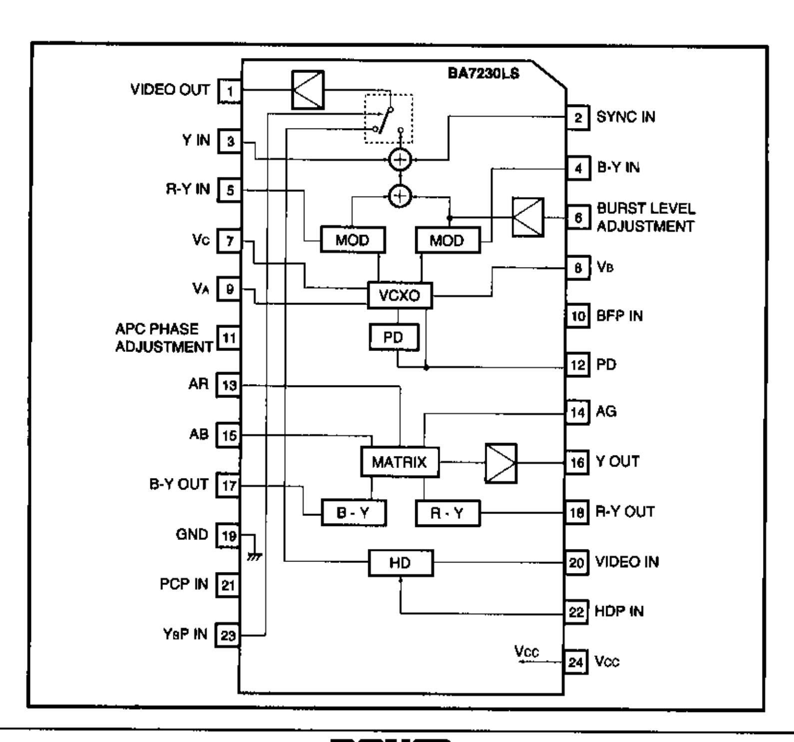
●Applications

Televisions (Teletext-capable), captain systems, video cameras, personal computers

●Features

1) Allows superimposition of video images (VIDEO IN) and computer images (RGB IN).
2) During superimposition, the subcarrier locked onto the video input burst signal RGB is modulated with the RGB signals by the APC circuit, preventing unnatural color disturbance due to switching.
3) Both the RGB and video input signals are pedestal-clamped, maintaining a natural image even during fluctuation in luminosity.
4) Using a half down pulse, the video signal can be reduced by 5dB to darken the background and make the superimposed RGB image easier to see.
5) Carrier leak is suppressible to less than $70mV_{P-P}$ (V_{OUT} = $2V_{P-P}$) without adjustment.
6) Can be adapted for analog RGB input.
7) Compact 24-pin SZIP package minimizes external components.

●Block diagram



● Pin input / output circuits

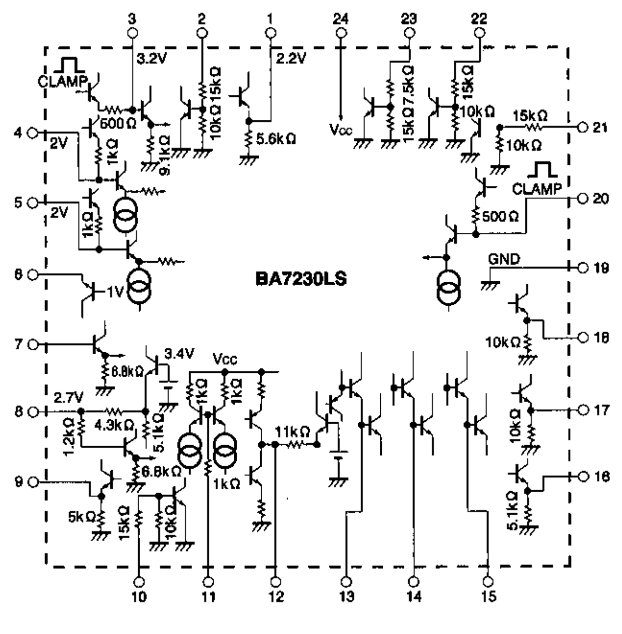


Fig. 1

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	7.0	V
Power dissipation	Pd	500*	mW
Operating temperature	Topr	−20~+70	°C
Storage temperature	Tstg	−55~+125	°C

* Reduced by 5.0 mW for each increase in Ta of 1°C over 25°C.

● Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	4.5~5.5	V
R input level	V_R	0~0.7	V_{P-P}
G input level	V_G	0~0.7	V_{P-P}
B input level	V_B	0~0.7	V_{P-P}
Video input level	V_{IN}	0~1.0	V_{P-P}

●Electrical characteristics (unless otherwise specified, Ta=25℃, V_{CC}=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Quiescent current	I_Q	−	38	54	mA	−	Fig.2
Video output level	V_{OV}	1.7	2.2	2.6	V_{P-P}	VIDEO IN=1V_{P-P}	Fig.2
Half down level change	G_{VH}	−3	−5	−7	dB	−	Fig.2
DC offset	V_{OF}	−	50	160	mV_{P-P}	VIDEO IN=1V_{P-P}	Fig.2
Crosstalk	CT	−	−46	−40	dB	VIDEO IN=1V_{P-P}	Fig.2
ER-EY output level	V_{R-Y}	0.3	0.42	0.55	V_{P-P}	V_R=0.7V_{P-P}	Fig.2
EB-EY output level	V_{B-Y}	0.2	0.31	0.42	V_{P-P}	V_B=0.7V_{P-P}	Fig.2
YOUT output level	V_Y	1.0	1.4	1.8	V_{P-P}	V_R=V_G=V_B=0.7V_{P-P}	Fig.2
Ys switching delay time	T_D	−	60	−	ns	−	Fig.2
SYNC output level	V_{OS}	0.4	0.65	0.9	V_{P-P}	−	Fig.2
Burst output level	V_{OB}	0.25	0.46	0.8	V_{P-P}	R_E=1.8kΩ	Fig.2
Composite output level	V_{OY}	1.7	2.2	2.6	V_{P-P}	Y_{IN}=0.7V_{P-P}	Fig.2
R-Y modulation gain	G_{R-Y}	9	11	13	dB	R - Y_{IN}=0.3V_{P-P}	Fig.2
B-Y modulation gain	G_{B-Y}	9	11	13	dB	B - Y_{IN}=0.2V_{P-P}	Fig.2
(R-Y) / (B-Y) modulation gain differential	G_{R-B}	−	−	2	dB	Difference between above gains	Fig.2
(R-Y) / (B-Y) orthogonal phase shift	ΔR	−6	−	6	deg	−	Fig.2
(R - Y) ·Burst orthogonal phase shift	ΔB	−6	−	6	deg	−	Fig.2
Carrier leak	L_{SC}	−	30	70	mV_{P-P}	V_{OUT}=2V_{P-P}	Fig.2
APC capture range	f_{CAP}	±100	−	−	Hz	Burst=0.1V_{P-P}, 2.8μS	Fig.2
Carrier phase range	ϕ_{SC}	±30	±45	−	deg	Superimposition	Fig.2
Video frequency characteristic	fv	4.5	6	−	MHz	-3 dB when f = 100 kHz	Fig.2
Video output DG	DG	−	±3.5	−	%	VIDEO IN=1V_{P-P}	Fig.2
Video output DP	DP	−	±2.5	−	deg	VIDEO IN=1V_{P-P}	Fig.2
Input impedance (SY, BF, PC, HD)	Z_T	8	15	−	kΩ	−	Fig.2
Input impedance (Ys)	Z_{TY}	3	7.5	−	kΩ	−	Fig.2
Threshold level (SY, BF, PC, HD)	V_T	0.9	2.0	2.8	V	−	Fig.2
Threshold level (Ys)	V_{TY}	0.5	1.1	1.8	V	−	Fig.2

●Measurement circuit

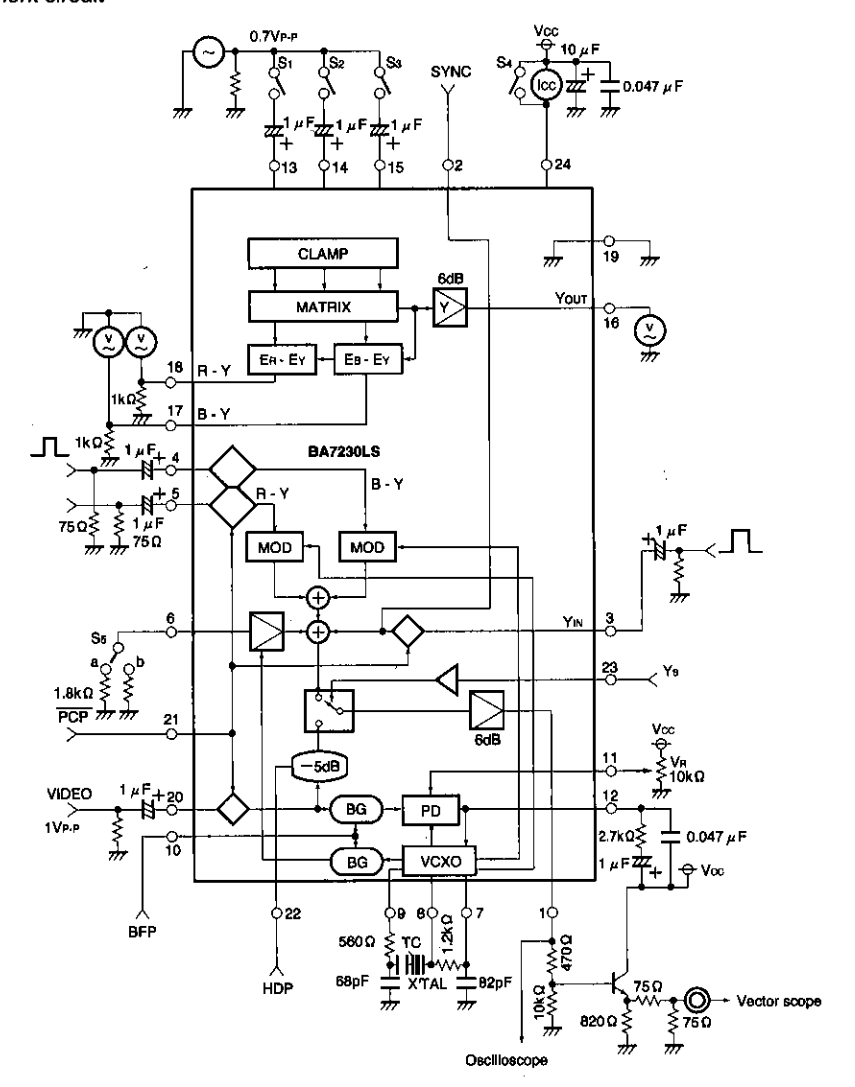
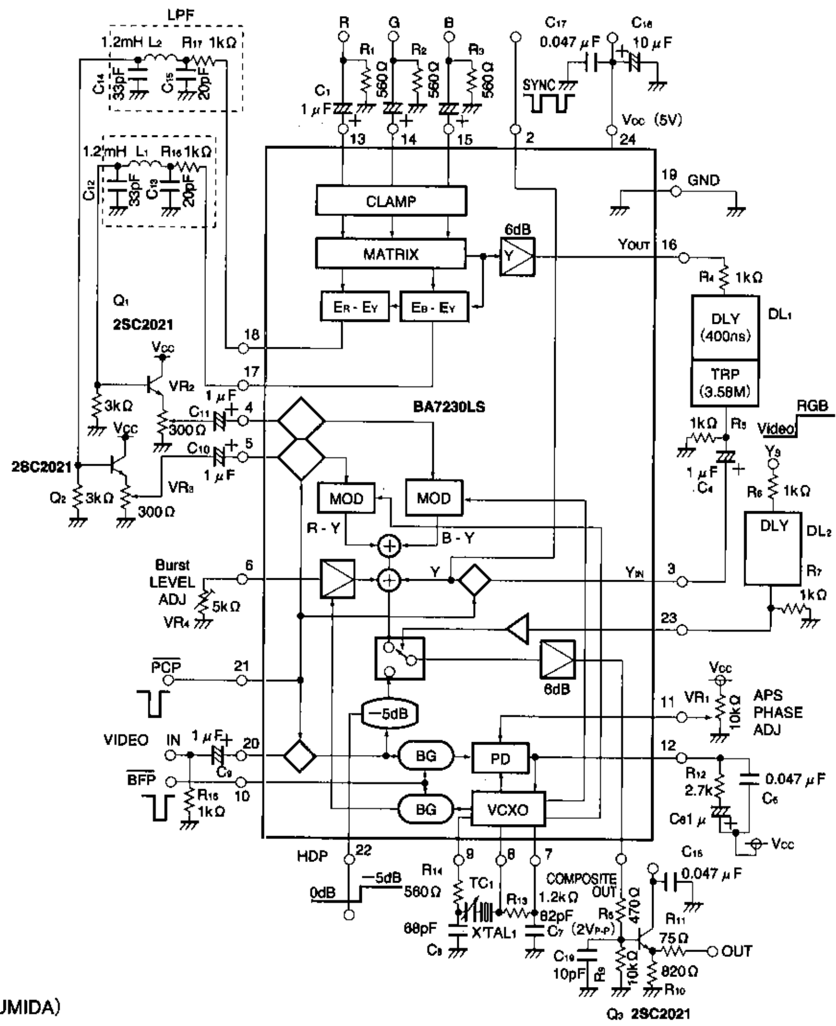


Fig. 2

●Application example



DL₁, DL₂ : X503 (SUMIDA)

L₁, L₂ : RC-875 1.2mH (SUMIDA)

TC₁ : TZ03R200E (MURATA)

Q₁, Q₂, Q₃ : 2SC2021 (ROHM)

XTAL₁ : HC−43U 3579.545kHz (NIKKO DENSHI)

Fig. 3

● Circuit operation

1) Matrix circuit

The R, G and B inputs are clamped to 3.2V by the clamp circuit and combined into signals E_Y, E_R-E_Y and E_B-E_Y by the resistance-adding matrix circuit.

$E_Y = 0.30E_R + 0.59E_G + 0.11E_B$

$E_R - E_Y = 0.70E_R - 0.59E_G - 0.11E_B$

$E_B - E_Y = -0.30E_R - 0.59E_G + 0.89E_B$

Signal E_Y is then amplified by the 6dB amplifier (pin 16) to compensate for the signal's 6dB attenuation in the delay line. To prevent overmodulation, signal E_R-E_Y is output at 1/1.14 and signal E_B-E_Y at 1/2.03 (pins 17 and 18).

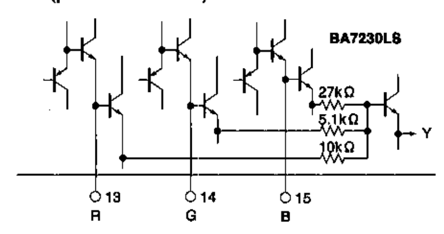


Fig. 4

2) Balanced modulator circuit

Color difference signals are modulated (rectangular 2-phase balanced modulation) with color subcarriers (3.58MHz) having a 90° phase difference. This is called the carrier color signal.

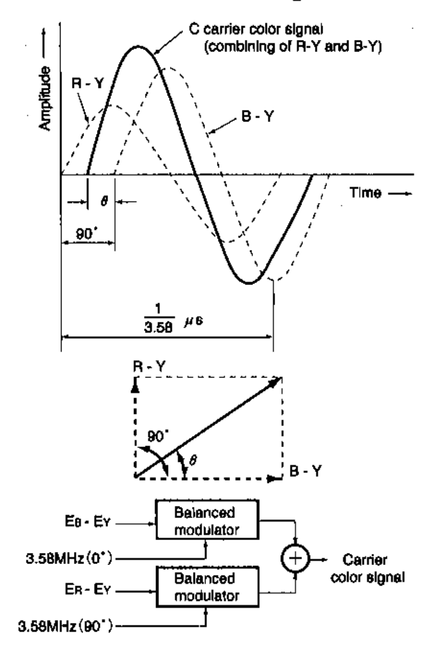


Fig. 5

The carrier color signal is mixed with color burst signals and luminosity signals E_Y (to which a horizontal synchronization signal is added) to create the NTSC composite signal (E_N).

$$E_N - E_Y + \frac{E_B - E_Y}{1.14}\cos 2\pi f_s t + \frac{E_B - E_Y}{2.03}\sin 2\pi f_s t$$

3) Switch circuit

Signal Ys (pin 23) switches between video input and RGB composite signals. Performing this switching at high speeds results in superimposition.

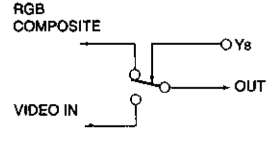


Fig. 6

4) Color subcarrier oscillator circuit

The subcarrier oscillator circuit for RGB input. This circuit is synchronized with the video input color burst signal extracted by $\overline{BFP}$ (burst flag pulses) during superimposition, preventing any unnatural color disturbance due to switching between RGB and video input.

This oscillator circuit generates the RGB color burst signal. An attached variable resistor can be used to change the amplitude of the color burst signal and to adjust its phase relative to the video color burst signal. This oscillator circuit remains in the free-running state when there is no video input.

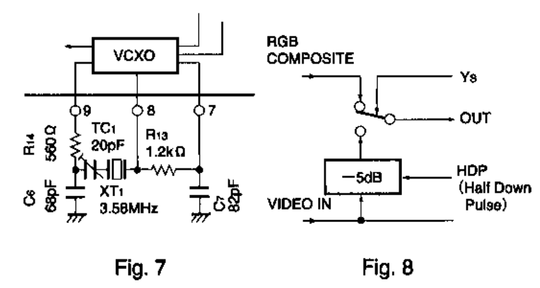


Fig. 7 Fig. 8

5) During superimposition, video input can be lowered by about 5dB using an HDP (half-down pulse), darkening the background and making RGB input easier to see.

● Input waveform and timing chart

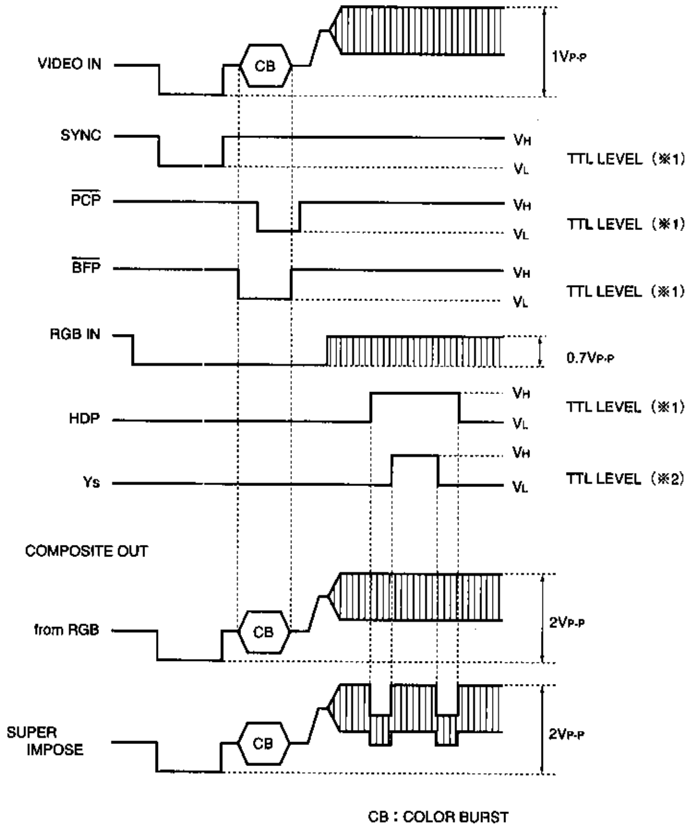


Fig. 9

●Operation notes

1) RGB and video inputs should be synchronized. When only RGB is input, connect VIDEO IN (pin 20) to GND with a 1 μF capacitor, and synchronize $\overline{PCP}$ and $\overline{BFP}$ to RGB.
2) Input pins with pedestal clamps cannot be left open and must be grounded with a low impedance. When not used, ground with a 1 μF capacitor.
※Input pins with pedestal clamps :
Y_{IN} (pin 3), B-Y_{IN} (pin 4), R-Y_{IN} (pin 5), VIDEO IN (pin 20)

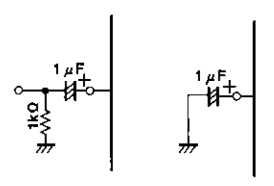


Fig. 10

3) The VCXO remains in a free-running state except during superimposition.
4) Pin 4 (B-Y_{IN}) and pin 5 (R-Y_{IN}) have high impedance and are susceptible to the effects of noise and other external factors during pattern generation. For this reason, we recommend adding the circuit in Fig. 11 to lower the input impedance. Adding this circuit can also reduce carrier leakage.

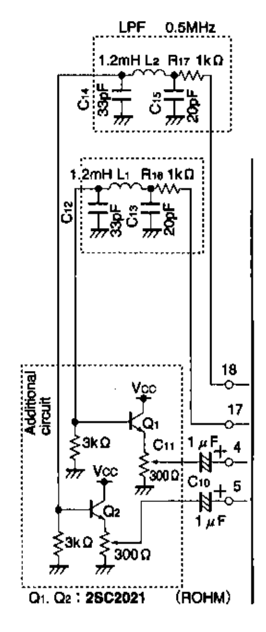


Fig. 11

●Electrical characteristic curves

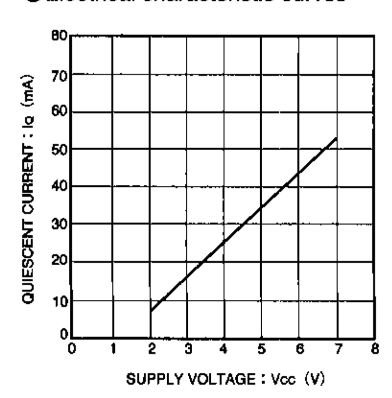


Fig. 12 Quiescent current vs. supply voltage characteristic

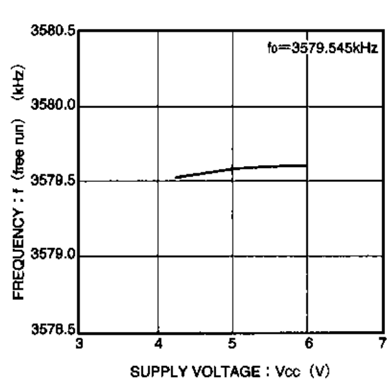


Fig. 13 VCXO free-run frequency vs. supply voltage characteristic

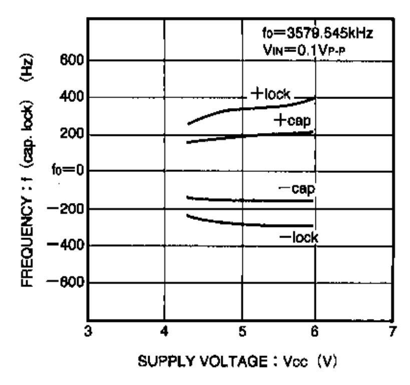


Fig. 14 Capture range and lock range (I) vs. supply voltage characteristic

Analog NTSC/PAL encoders
Multimedia video

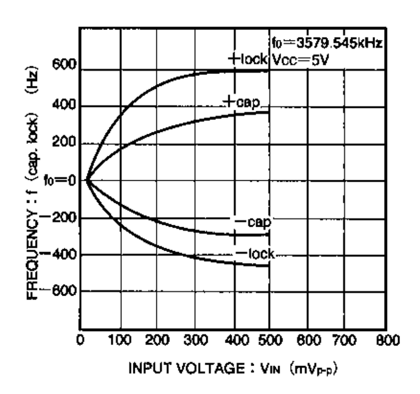
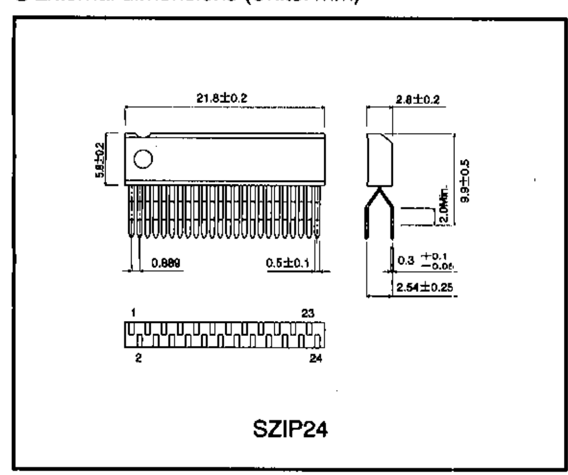


Fig. 15 Capture range and lock range (II) vs. input voltage characteristics

●External dimensions (Units: mm)



SZIP24